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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/823,544

04/14/2004

Wong-Sang Song

253/007 DIV

4407

27849

7590

03/29/2007

LEE & MORSE, P.C.

3141 FAIRVIEW PARK DRIVE

SUITE 500

FALLS CHURCH, VA 22042

EXAMINER

QUACH, TUAN N

ART UNIT

PAPER NUMBER

2826

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

03/29/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/823,544

Applicant(s)

SONG ET AL.

Examiner

Tuan Quach

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14 and 16-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 and 16-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☒ Certified copies of the priority documents have been received in Application No. 09/949,853.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

  
**Tuan Quach**  
**Primary Examiner**

## DETAILED ACTION

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. '357 taken with Besser et al. and either Lin et al. 5,010,037 or Thakur.

Re claim 18, Lin et al. 6,316,357 B1 teach semiconductor device having a metal silicide contact structure comprising silicon substrate 52, gate oxide 64 thereon, gate stack 62 including polysilicon thereon, a metal silicide layer 76/80/82/84 formed on the directly on the gate and substrate including desired thickness less than 100 angstroms. Re claim 19, the respective source drain and lightly doped source drain and gate spacers are also shown, regions, 54/56/58/60, and 66/68. See Fig. 2D, 3D, column 5

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line 35 to column 7 line 16, column 10 lines 13-19. Lin et al. lack primarily the showing of a silicon containing capping layer.

Besser et al. 5,970,370 teach the use of a capping layer e.g., 403, Fig. 3A, on metal 402 for fabrication of silicide structures having small feature sizes and linewidths. See the abstract, column 3 line 20-38, column 4 line 48 to column 7 line 45.

Lin et al. '037 further teaches the use of capping comprising silicon layer 16 (which subsequently conductive or crystalline 16') on silicide 14', (including very thin silicide, column 3 lines 10-12) having improved characteristics, e.g., pinholefree, see abstract, column 2 lines 30-57, column 3 lines 10-65.

Thakur 2002/0006722 also teaches capping layer 25 containing silicon including conductive polysilicon on silicide 24 to obtain smooth surface, reduced reflectivity, among other improved characteristics. See abstract, [0016], [0022]

It would have been obvious to one skilled in the art in practicing the above invention to have employed the capping layer since such is conventional and advantageous as taught by Besser et al. to obtain silicides having desired characteristics as taught by Besser et al. Conversely, the use of silicide layer less than 100 angstroms would have been apparent or inherent in Besser, e.g., using cobalt of 50 angstroms or above, (the same or similar thickness employed in the instant application [0034], [0035], [0056], etc.); or otherwise such would have been conventional and within the purview of one skilled in the art given the thickness in Lin as delineated. The use of capping layer including silicon on silicide is conventional and advantageous as taught by Lin et al. '037 or Thakur above and as such would have

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been obvious. The recitation regarding the silicide containing from both silicon containing substrate and silicon containing conductive layer is inherently met in Lin et al. '037 as shown above and as in Thakur above wherein the polysilicon is not prevented from diffusion into the silicide. Such would not further impart patentability into the claims since it does not correspond to a difference in structural limitations but rather corresponding to a product by process limitation, note that a "product-by-process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and the related case cited therein which make it clear that it is the final product per se which must be determined in a "product-by-process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product-by-process" claims or not. As stated in *Thorpe*,

Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA, 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969).

When the prior art discloses a product which reasonably appears to be either identical with or only slightly different than a product claimed in a product-by-process claim, a rejection based alternatively on either section 102 or section 103 of the statute is eminently fair and acceptable. As a practical matter, the Patent Office is not equipped to manufacture products by the myriad of processes put before it and then obtain prior art products and make physical comparisons therewith." *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972).

"The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. *In re Fessmann*, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art,

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although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. In re Marosi, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983)

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Besser et al. in view of Lin et al. '037 or Thakur.

Besser et al. 5,970,370 as applied above which shows substrate, including silicon substrate, gate oxide 821, gate 822 including polysilicon as newly claimed, metal silicide 1010, capping layer 403. The silicide thickness would be less than 100 angstroms, given the thickness of cobalt employed, e.g., 50 angstroms or so, see Fig. 8-12, column 6 line 40 to column 9 line 30, consistent with similar thicknesses employed in the instant application as delineated above. Alternatively, the selection of suitable and desired thickness less than 100 angstroms for the silicide would have been within the purview of one skilled in the art and as such would have been obvious. Besser et al. lack primarily the recitation of silicon containing capping.

Lin et al. '037 or Thakur are applied above. Lin et al. '037 further teaches the use of capping comprising silicon layer 16 (which subsequently conductive or crystalline 16') on silicide 14', (including very thin silicide, column 3 lines 10-12) having improved characteristics, e.g., pinholefree, see abstract, column 2 lines 30-57, column 3 lines 10-65.

Thakur 2002/0006722 also teaches capping layer 25 containing silicon including conductive polysilicon on silicide 24 to obtain smooth surface, reduced reflectivity, among other improved characteristics. See abstract, [0016], [0022]

It would have been obvious to one skilled in the art to have employed the use of capping layer including silicon on silicide which is conventional and advantageous as taught by Lin et al. '037 or Thakur above and as such would have been obvious. The recitation regarding the silicide containing from both silicon containing substrate and silicon containing conductive layer is inherently met in Lin et al. '037 as shown above and as in Thakur above wherein the polysilicon is not prevented from diffusion into the silicide. Such would not further impart patentability into the claims since it does not correspond to a difference in structural limitations but rather corresponding to a product by process limitation, note that a "product-by-process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and the related case cited therein which make it clear that it is the final product per se which must be determined in a "product-by-process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product-by-process" claims or not. As stated in *Thorpe*,

Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA, 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969).

When the prior art discloses a product which reasonably appears to be either identical with or only slightly different than a product claimed in a product-by-process claim, a rejection based alternatively on either section 102 or section 103 of the statute is eminently fair and acceptable. As a practical matter, the Patent Office is not equipped to manufacture products by the myriad of processes put before it and then obtain prior art products and make physical comparisons therewith." *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972).

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"The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. In re Fessmann, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. In re Marosi, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983)

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Besser et al. and either Lin et al. '037 or Thakur as applied to claim 18 above, and further in view of Lin et al. '357.

Besser et al., Lin et al. '037, Thakur as applied above; Besser et al. also show spacers 825 but does not necessarily or explicitly recite the lightly doped source drain. It would have been obvious to one skilled in the art in practicing the above invention to have included the lightly doped source drain regions since such correspond to notoriously conventional structures as taught in Lin et al. 6,316,357 supra, column 5 lines 36-39.

Claims 1-12, 16 are rejected under 35 U.S.C. 103(a) as being obvious over Besser et al. in view of Lin et al. '037 or Thakur.

Re claim 1-12, ~~45~~, 16, Besser et al. and Lin '037 or Thakur are applied as above. The silicide thickness would be less than 100 angstroms, given the thickness of cobalt employed, e.g., 50 angstroms or so, see Fig. 8-12, column 6 line 40 to column 9 line 30, consistent with similar thicknesses employed in the instant application as delineated above. Alternatively, the selection of suitable and desired thickness less



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than 100 angstroms for the silicide would have been within the purview of one skilled in the art and as such would have been obvious.

Besser et al. additionally shows the application of an insulation 1301 having opening 1302 on substrate, metal silicide 1010d in the opening and conductive thereon are shown in Fig. 14, column 7 lines 30-45. Re claim 2, conductive layer of silicon is taught, column 7 line 45. Re claim 3, the two phases of silicides correspond to the cobalt monosilicide and disilicide taught at column 7 lines 1-25, column 5 line 1-38. Re claim 4, silicon substrate is shown column 5 line 45; alternatives SOI, SiGE, etc. correspond to notoriously conventional substrate materials and otherwise would have been obvious; alternatively, official notice is given regarding such notoriously conventional material. Re claims 5-7, the use of polysilicon layer on the structure is shown above, column 7 line 45 and the use of alternative semiconductor material, would have been obvious as delineated above; alternatively, official notice is given regarding such material. Re claim 7, the resistivity would have been inherent and obvious as shown in Fig. 2. Re claims 9-12, the conventional structures of gate oxide, gate, spacers, source drains are shown as delineated above, Figs. 8-12. Re claim 15, the capping layer of titanium nitride is taught above, layer 403, column 6 line 40 to column 9 line 30. The metallic material for the conductive layer in claim 16 is shown, column 9 line 45. Besser et al. lack primarily the recitation of the silicon containing capping.

Lin et al. '037 or Thakur are applied above. Lin et al. '037 further teaches the use of capping comprising silicon layer 16 (which subsequently conductive or crystalline

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16') on silicide 14', (including very thin silicide, column 3 lines 10-12) having improved characteristics, e.g., pinholefree, see abstract, column 2 lines 30-57, column 3 lines 10-65.

Thakur 2002/0006722 also teaches capping layer 25 containing silicon including conductive polysilicon on silicide 24 to obtain smooth surface, reduced reflectivity, among other improved characteristics. See abstract, [0016], [0022]

It would have been obvious to one skilled in the art to have employed the use of capping layer including silicon on silicide which is conventional and advantageous as taught by Lin et al. '037 or Thakur above and as such would have been obvious. The recitation regarding the silicide containing from both silicon containing substrate and silicon containing conductive layer is inherently met in Lin et al. '037 as shown above and as in Thakur above wherein the polysilicon is not prevented from diffusion into the silicide. Such would not further impart patentability into the claims since it does not correspond to a difference in structural limitations but rather corresponding to a product by process limitation, note that a "product-by-process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and the related case cited therein which make it clear that it is the final product per se which must be determined in a "product-by-process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product-by-process" claims or not. As stated in *Thorpe*,

Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d

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531, 535, 173 USPQ 685, 688 (CCPA, 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969).

When the prior art discloses a product which reasonably appears to be either identical with or only slightly different than a product claimed in a product-by-process claim, a rejection based alternatively on either section 102 or section 103 of the statute is eminently fair and acceptable. As a practical matter, the Patent Office is not equipped to manufacture products by the myriad of processes put before it and then obtain prior art products and make physical comparisons therewith." *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972).

"The Patent Office bears a lesser burden of proof in making out a case of *prima facie* obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. *In re Fessmann*, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. *In re Marosi*, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983)

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Besser et al. taken with Lin et al. '037 or Thakur as applied to claims 1-12, 16 above and further in view of Hada et al.

Regarding the alternative material of silicon germanium or germanium, such use is conventional as evidenced by Hada et al. 5,909,059 the abstract to obtain low resistance material. Crystalline or amorphous correspond to two obvious and conventional forms of the semiconductor and its use is notoriously conventional and obvious.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Besser et al. taken with Lin et al. '037 or Thakur as applied to claims 1-12, 16 above and further in view of Hyakutake.

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Regarding claim 17, although the prior art above does not show the additional metal, such is well known as evidenced by Hyakutake, 6,087,250 the abstract and Fig., layer 7A/7B above the plug 4 wherein multilevel interconnection can be made.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Besser et al. taken with Lin et al. '037 or Thakur as applied to claims 1-12, 16 above and further in view of Nam and Lee.

Besser et al. and Lin et al. and Thakur are as applied above, Besser does not explicitly recite the pad layer or the bit line stack in claim 13 and 14.

Nam 6,133,109 shows conventional DRAM cell capacitor including pad 104 between field oxide 102 prior to forming additional insulation 106a, bit line 108, insulation 106, and conductive layer 114 for storage electrode contacting the pad 104. See Figs. 3, 7B, 9 column 3 line 38-55, column 8 lines 43-62.

Lee 6,168,992 B1 also shows pad 106a between field oxide 102, second insulation 108, bit line 110, additional insulations, 116-124, conductive 126 to permit formation DRAM devices and storage electrode connection. See Figs. 1D-1E column 3 line 30 to column 5 line 35.

It would have been obvious to one skilled in the art in practicing the above invention to have included such conventional structures for applications in DRAM cell capacitor and storage electrode connections as taught by Nam and Lee above..

Applicant's arguments with respect to claims 1-14 and 16-19 have been considered but are moot in view of the new ground(s) of rejection.

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Tuan Quach whose telephone number is 571-272-1717. The examiner can normally be reached on M-F from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**Tuan Quach**  
**Primary Examiner**